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Total Harmonic Distortion (THD) Analysis of 5-Level and 7-Level Cascaded Multilevel Inverters at Different Switching Frequencies

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Abstract*—Multilevel inverters convert DC voltage to AC voltage by using lower DC voltage at the input, with the help of an electronically controlled device. One of the primary challenges linked to these devices is the Total Harmonic Distortion (THD) present in the output waveforms. In this research paper, concise overview of Total Harmonic Distortion (THD) is presented for different cascaded H-bridge multilevel inverter topologies, in particular, the five-level and seven-level inverters illustrate this concept well. The five-level inverter employs eight switches, whereas the seven-level inverter uses twelve switches. Each H-bridge inverter circuit operates with separate DC sources. The inverter employs an Insulated Gate Bipolar Transistor (IGBT) serves as the switching component and a gating block to regulate the operation of the IGBT switching. Simulation results and waveform analysis are provided to confirm the research findings. The study also explores the effect of varying the switching frequency of the carrier wave on the total harmonic distortion of the output waveforms. The paper highlights the significance of choosing the right switching frequency according to application requirements to enhance the performance and efficiency of cascaded multilevel inverters.

Keywords*— Multilevel inverters, Total Harmonic Distortion, cascaded H-bridge multilevel inverter topologies, single H-bridge inverter circuit, independent DC sources, waveform analysis

I. Introduction

Multilevel inverters are electronic devices which can generate the required alternating voltage at the output by using reduced DC voltages as input. Typically, solar cells, fuel cells or batteries are used as input sources. A two-level inverter is frequently utilized to convert DC voltage into AC voltage, but its waveform is non-sinusoidal and contains harmonics. To address the drawbacks of the conventional two-level inverter, such as low efficiency, high cost and switching losses, multilevel inverters have been introduced. Multilevel inverter systems are capable of generating a pure sinusoidal waveform of various levels at the output voltage, as illustrated in Fig. (1), this topology is gaining popularity due to its high voltage operating capabilities, relatively low switching losses, high efficiency, and minimal Electromagnetic Interference (EMI). It has received significant attention across multiple disciplines in recent years because of its capability to produce output voltage with lower Total Harmonic Distortion (THD) and minimized harmonics while decreasing the percentage of losses. The multilevel inverter topology is designed to generate an AC source that closely resembles a pure power generation source and can be utilized for AC loads. Increasing the levels of the inverter circuit allows for the generation of a smoother waveform The greater the number of levels, the smoother the output voltage waveform will be [1,2,3].

Multilevel inverters can be classified into two main types based on the type of DC sources: separate DC sources. and common dc source, the first type is divided to cascaded inverters and flying capacitors. The second type uses diode-clamped inverters. The cascaded H-bridge inverter is popularly used for single-phase systems.

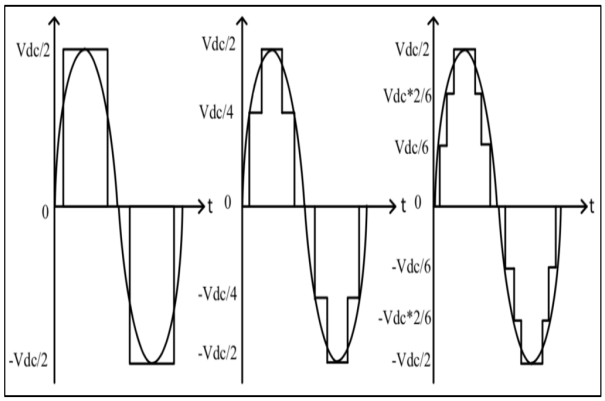


Fig. 1 Output voltage waveform for 3-level, 5 level, 7 levels of multilevel inverters [2].

The PWM-based technique can give a better dynamic response in addition to the lower THD of output voltage and current. The difference between the several topologies of multilevel inverters available in the mechanism of switching and the source of input voltage to the multilevel inverters. The three most commonly used multilevel inverter topologies are

cascaded bridge multilevel inverters, Diode Clamped multilevel inverters and Flying Capacitor multilevel inverters. Among these three Cascade H-bridges multilevel has a modular structure and requires fewer components than diode clamped and flying capacitor multilevel inverter, and consequently, it is widely used for many applications. The key features of multilevel inverters are as follows [4, 5]:

1. The output voltage and power increase with the number of levels.

2. The harmonic content is inversely proportional to the number of levels, reducing the need for filtering.

3. Specific harmonics can be targeted for elimination, as higher voltage levels provide more available switching angles.

4. Switching devices can handle both static and dynamic voltage sharing, with clamping diodes or capacitors aiding in this process.

5. Voltage-sharing issues are not encountered by the switching devices [6, 7].

This paper mainly focuses on the Simulation results of five-level and seven-level single-phase cascaded H-bridge multilevel inverters and the effects of the switching frequency on their THD values are presented.

II. CSCADED H-BRIDGE MULTILEVEL INVERTER

The cascaded multilevel inverter (CMI) with isolated DC sources is regarded as the most feasible topology for power conversion in medium and high-power applications. This is due to its ability to eliminate the need for bulky transformers, clamping diodes, and flying capacitors that are required by conventional multilevel inverters, diode-clamped multilevel inverters, and flying-capacitor multilevel inverters, respectively To achieve m levels, where m = (2n+1), each phase of the cascaded multilevel inverter requires number of DC sources equal n. The power circuit of the IGBT-based PWM multilevel inverter is shown in Fig. (2) which consists of 2(m-1) IGBTs. Each independent DC source is connected to a single-phase full-bridge inverter. The AC output voltages of the different level inverters are cascaded in series. By utilizing different combinations of the four switches, S1-S4, each inverter level is capable of generating three distinct voltage outputs: +Vdc, -Vdc, and zero. The AC outputs of the multiple full-bridge converters in the same phase are connected in series, producing a combined voltage waveform that represents the sum of the outputs from each individual converter [8].

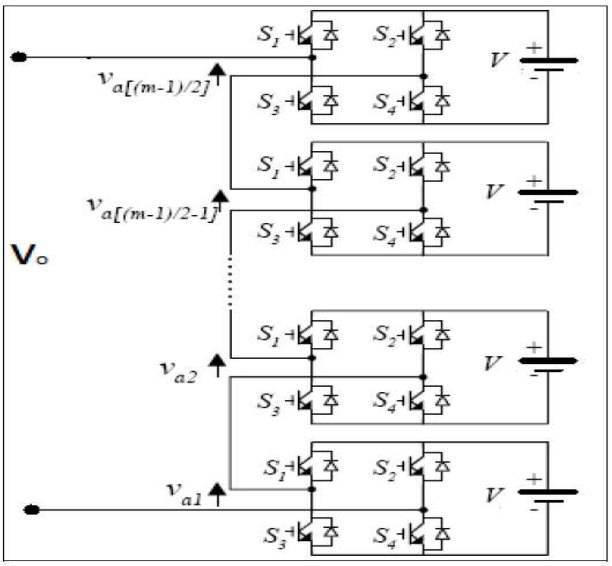


Fig.2 Single phase five-level configuration of cascaded H- bridge inverter

A) Methodology of THD Reduction

The operation of various multilevel inverters at different switching frequencies is carried out using MATLAB Simulink. Among the different multilevel inverters, the five-level and seven-level inverter topologies are introduced. In this paper, the Total Harmonic Distortion (THD) of five-level and seven-level multilevel inverters can be minimized by adjusting the switching frequency of the carrier signals used in the PWM method. The PWM method is utilized to generate the necessary gate pulses for the switching devices. This approach requires fewer components and helps reduce lower-order harmonics. Higher-order harmonics can be minimized by incorporating filter circuits. Essentially, in the sinusoidal PWM technique, there are two signals: the reference signal (a sinusoidal wave) and the carrier signal (a triangular wave) of a higher frequency. These signals are compared to produce the ON and OFF states. The output voltage magnitude can be controlled by adjusting the modulation index (Ml). For an m-level inverter, triangular waves numbering (m−1) are compared with a sinusoidal wave.

B) Total Harmonic Distortion (THD) Calculation

The total harmonics distortion (THD) is mathematically given by

$$D = \frac{\sqrt{\sum_{n=2}^{\infty} H(n)^2}}{H1} \qquad (1)$$

Where: $H1$ is the amplitudes of the fundamental component, whose frequency is ω_0 and $H(n)$ is the amplitudes of the nth harmonics at $n\omega_0$.

The amplitude of the fundamental and harmonic components of the quarter-wave symmetric multilevel waveform can be express as:

$$h_n = \frac{4E}{n\pi} \sum_{k=1}^{S} cos(n\alpha_k) \qquad (2)$$

Let $H_{(n)}=h_n$ and $H_1=h_1$

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} h_{\cdot} n^2}}{h_1} \qquad (3)$$

$$THD = \frac{\sqrt{\sum_{n=}^{\infty}(\frac{1}{n}\sum_{k=1}^{s} Cos(n\propto_k)^2}}{\sum_{k=1}^{s} Cos(\propto_1)} \quad (4)$$

Therefore, the output voltage THD of the given waveform can be calculated. Theoretically, to obtain the exact THD, an infinite number of harmonics would need to be considered. However, this is not feasible in practice. Consequently, a specific number of harmonics will be used, depending on the desired precision of the THD calculation. Typically, a limit of 63 harmonics is generally accepted.

III. SINUSOIDAL PWM TECHNIQUE

This technique involves producing pulses of varying widths during each half-cycle, with the pulse width being a sinusoidal function of the angular position within each cycle. To accomplish this, a triangular wave is compared to a sinusoidal waveform that has the same frequency as the input voltage, as illustrated in Fig. (3). The type of pulse width modulation (PWM) and the number of pulses per half-cycle can be modified to eliminate or reduce lower-order harmonics. While higher-order harmonics may increase, they can be effectively eliminated using filters. The number of pulses per cycle is determined by the ratio of the triangular carrier frequency to the modulating sinusoidal frequency. The modulation index is represented by the following equation:

Modulation index = A_r/A_c where, (5)

A_r: is the amplitude of reference waveform and,

A_c is the amplitude of carrier waveform.

In case of multilevel inverter the number of carrier signals is determined by the number of output-phase voltage levels.

N_c =N-1 where

N_c: number of carrier signals

N: number of output- phase voltage levels

For seven level, six carrier signals are to be used, for nine levels, eight carrier signals are to be used and so on.

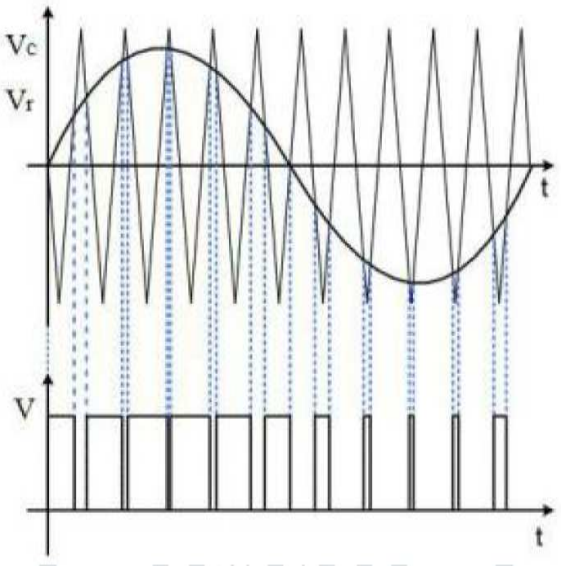


Fig.3 Concept of sinusoidal pulse width modulation

This method results in the generation of pulses with a constant width but varying amplitude. It involves comparing a reference sine wave with high-frequency triangular carriers. The instants of switching and commutation of the switches is determined by the points of crossroad of reference and carrier swells. For multilevel inverters, SPWM fashion is further classified as follows depending on the demand of multiple carrier signals [9,10].

1- Phase shifted pulse width modulation (PSPWM)
2- Level shifted pulse width modulation (LSPWM)
3- Phase disposition (PD)
4- Phase opposition disposition (POD)
5- Alternate phase opposition disposition (APOD) [11].

IV. HARMONIC REDUCTION TECHNIQUE

Multilevel inverters that use Carrier-based modulation schemes can be classified into two categories: phase-shifted modulation and level-shifted modulation. as illustrated in Fig. (4). Both modulation schemes can be applied to cascaded H-bridge inverters; however, the total harmonic distortion of phase-shifted modulation is higher than that of level-shifted modulation. Consequently, we have opted to use level-shifted modulation. To implement an m-level multilevel inverter using level-shifted multicarrier modulation, (m-1) triangular carriers with the same frequency and amplitude are needed. These (m-1) triangular carriers are positioned vertically so that the bands they occupy are contiguous.

The frequency modulation index, given by $m_f = f_{cr}/f_m$, remains the same as that for the phase-shifted modulation scheme, while the amplitude modulation index is defined as:

$$ma = \frac{Vm}{Vcr(m-1)} \quad \text{For } 0 < ma < 1 \quad (6)$$

Where Vm : is the peak amplitude of the modulating wave

Vcr : is the peak amplitude of each carrier wave.

The Level shifted pulse width modulation has three types named as:

1. In-Phase Disposition (IPD), where all carriers are synchronized in phase.
2. Phase Opposition Disposition (POD), where all carriers above the zero reference are in phase but opposite to those below the zero reference.
3. Alternate Phase Opposition Disposition (APOD), where all carriers are alternately arranged in opposition [12,13].

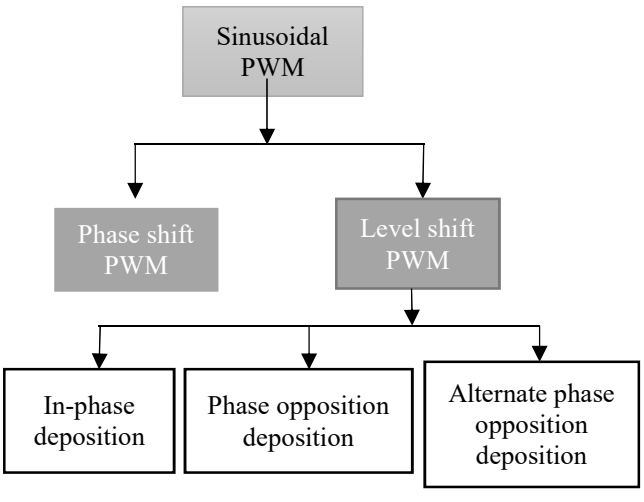


Fig.4 Classification of sinusoidal PWM used for multilevel inverter.

V. FIVE LEVEL CASCADED H-BRIDGE MULTILEVEL INVERTER

The five-level cascaded H-bridge inverter circuit consists of two individual H-bridge inverter circuits, as illustrated in Fig. (5). Each H-bridge circuit is supplied with a DC voltage input, resulting in two inputs (V1 and V2). Each H-bridge comprises four IGBTs, with a total of eight switches for the entire stage (S1, S2, S3, S4, S5, S6, S7, and S8) arranged in an H-shape configuration, and each IGBT is connected to a gating block for switching control. The cascaded H-bridge inverter circuit is powered by a 100V DC supply for each single H-bridge inverter circuit. Each IGBT is assigned individual gating parameters to facilitate switching operations and produce the appropriate output waveform pattern. To achieve the desired output voltage level in a five-level inverter, the switches are operated according to Table (1). From Table (1), it is clear that the 'ON' and 'OFF' states of the switches are represented by 0 and 1, respectively. In each output voltage phase of this inverter, four IGBTs must be turned 'ON' while the remaining four stay 'OFF' [14].

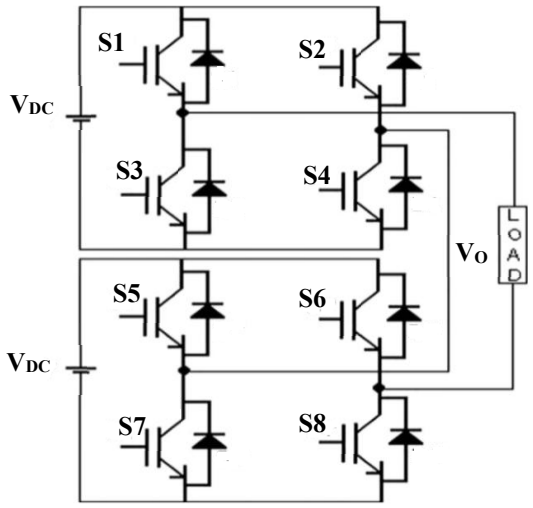


Fig. 5 Single phase structure of a five- level cascaded H-bridge inverter.

Table 1. output voltage levels for the five levels of multilevel inverter

S1	S2	S3	S4	S5	S6	S7	S8	Voltage level
0	1	1	0	0	1	1	0	$+V_{DC}$
1	1	0	0	0	1	1	0	$+2V_{DC}$
1	1	0	0	1	1	0	0	0V
1	1	0	0	1	0	0	1	$-2V_{DC}$
1	0	0	1	1	0	0	1	$-V_{DC}$

VI. SEVEN LEVEL CASCADED H-BRIDGE MULTILEVEL INVERTER

To generate the desired output waveform in a seven level cascaded H-bridge inverter, three separate H-bridge inverter circuits are utilized. circuits are required, as illustrated in Fig. (6). Each circuit is fed with an independent DC voltage source of the same magnitude (V1, V2, and V3) and consists of twelve IGBTs arranged in an H shape (S1-S12). The DC input voltage provided to each H-bridge cell is 100V, and each gating block generates a switching pattern as a waveform for the power IGBTs. The switching operations needed to achieve The output waveforms for the seven-level multilevel inverter are shown in Table (2). In this table, the 'ON' and 'OFF' states of the switches are represented by 1 and 0 Six switches will be engaged at the same time to generate the required level in each output voltage phase, respectively. It can be noted from the state changes that six switches will be active simultaneously to produce the necessary level in each output voltage phase [14].

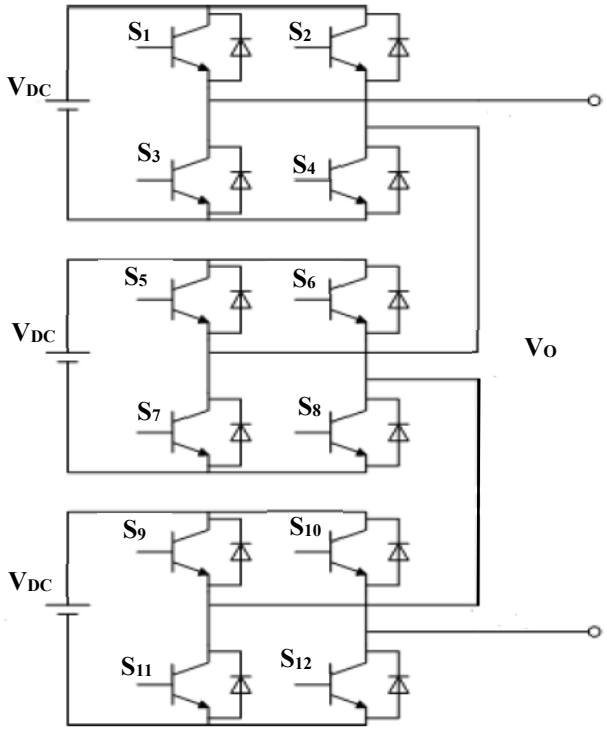


Fig.6 Single phase structure of a seven-level cascaded H-bridge inverter.

Table 2. output voltage levels for the seven levels of multilevel inverter

S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	Voltage level
1	0	0	1	1	0	0	1	1	0	0	1	$+3V_{DC}$
1	0	0	1	1	0	0	1	0	0	1	1	$+2V_{DC}$
1	0	0	1	0	0	1	1	0	0	1	1	$+V_{DC}$
0	0	1	1	0	0	1	1	0	0	1	1	0V
0	1	1	0	0	0	1	1	0	0	1	1	$-V_{DC}$
0	1	1	0	0	1	1	0	0	0	1	1	$-2V_{DC}$
0	1	1	0	0	1	1	0	0	1	1	0	$-3V_{DC}$

VII-ANALYSIS FOR SINGLE-PHASE CASCADED H-BRIDGE

To evaluate the capability of both the five-level and seven-level cascaded H-bridge inverters to generate all possible positive and negative levels symmetrically in the output voltage waveform, both were configured with different values of switching angles.

For simulation purposes, each DC voltage source is set to 100V, and the frequency of the output voltage is assumed to be 50Hz. The load resistance is 5 Ohm and 5mH inductance. Voltage of different levels (five and seven) are analyzed and For the calculation of harmonics, FFT analysis is utilized to determine the Total Harmonic Distortion (THD), which is presented for various cases of carrier frequency and different levels in the figures below [14].

(A) Output Voltage for Five Level and Seven Level Multilevel Inverter

The output voltage for the five-level and seven-level inverters is illustrated in Fig. (7) and Fig. (8), confirming that the inverter could generates all the required positive and negative levels symmetrically in output voltage waveform, each configured with different switching frequency values. The circuit simulation yielded a maximum output voltage of +200V and a minimum value of -200V, as illustrated in Figure (7) and Figure (8) shown, the maximum output voltage obtained from circuit simulation is +300V the minimum value is shown as -300V, as depicted. The output voltage waveform can be adjusted by setting the value of the input DC voltage. The configuration of this voltage determines the waveform's levels.

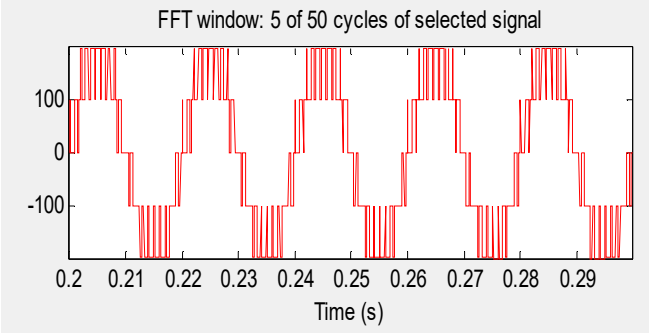


Fig. 7 The output voltage waveform for five -level inverter

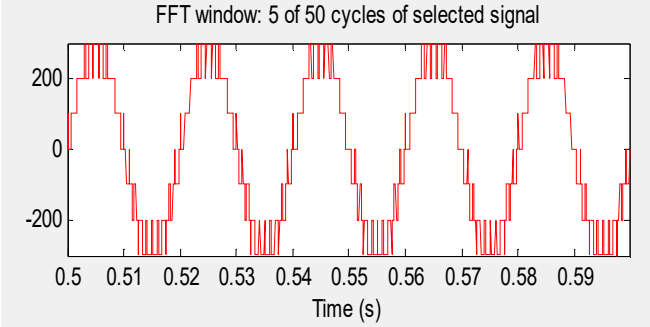


Fig. 8 The output voltage waveform for seven -level inverter

(B) THD in Five Level and Seven Level Multilevel Inverter at Different Switching Frequency.

Since the inverter aims to use a DC voltage source to supply the AC power needed by the load, the quality of the AC output voltage or current should be assessed based on THD From the simulated analysis, figure (9) show that at f=500Hz, THD is 26.2% as in Fig. (9.A), and at f=1000Hz, the THD is 24.92% as in Fig. (9.B), at f=1500Hz, THD is 21.45%, as in Fig.(9.C). These values indicate that the THD of the output voltage for the five-level inverter decreases as the switching frequency increases.

Figure (10) shows the THD for the output voltage of the seven-level multilevel inverter at switching frequencies of 500, 1000, and 1500, respectively .From this figure, we note that at f=500Hz, THD is 18.75% as shown in Fig(10.A), and at f=1000Hz, the THD is 16.06% as shown in Fig.(10. B), at f=1500Hz, THD is 14.05% as shown in Fig. (10.C). This values indicates that, the THD of the output voltage for the seven-level inverter reduces as the switching frequency rises. It can be deduced also that, for five level at f=500Hz, THD is 26.2$ but for seven level at the same frequency, THD is 18.57% and at f=1000Hz, THD for five level is 24.92%, but for seven level THD is 16.06%. At f=1500Hz, THD of five level is 21.45% and for seven level THD is 14.05%. At f=2000Hz, THD for five level is 18.95% and for seven level THD is 12.12%. At f=2500Hz, THD for five level is 16.13% but for seven level THD is 10.07%

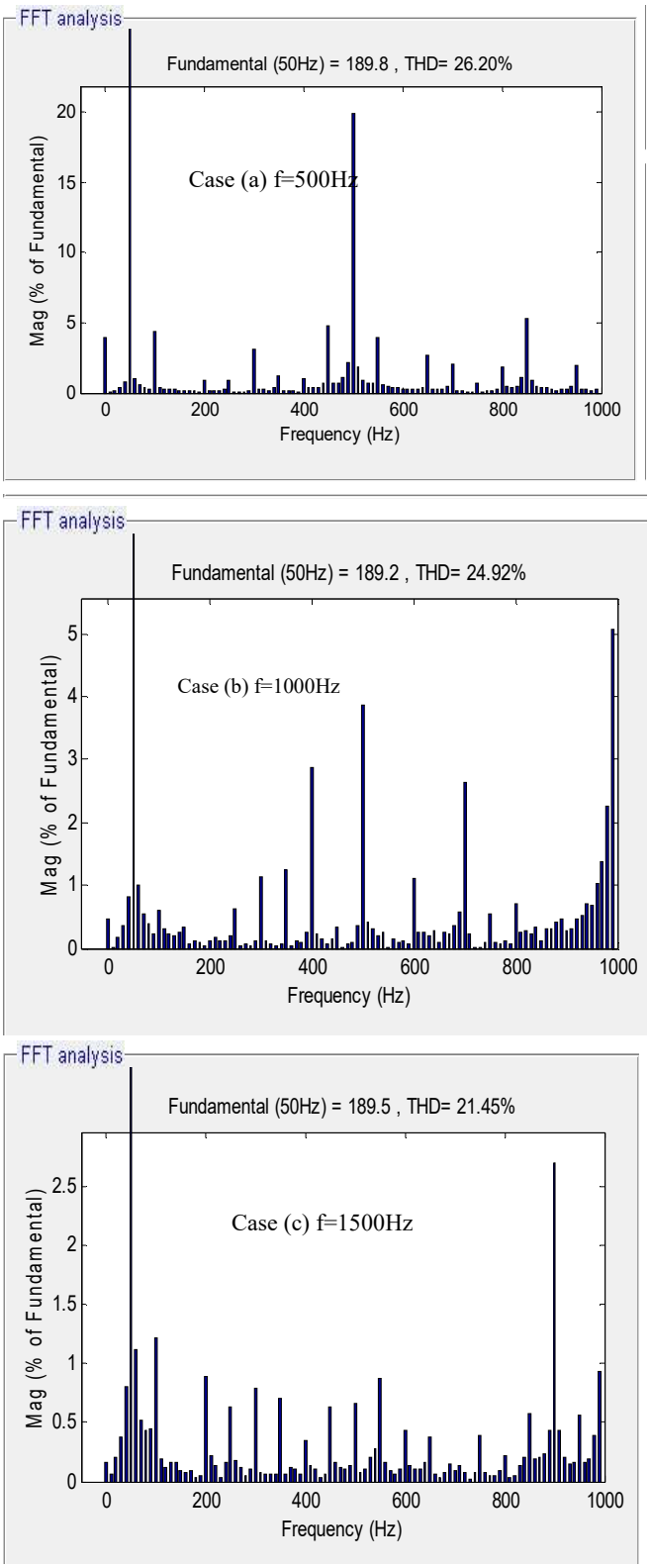
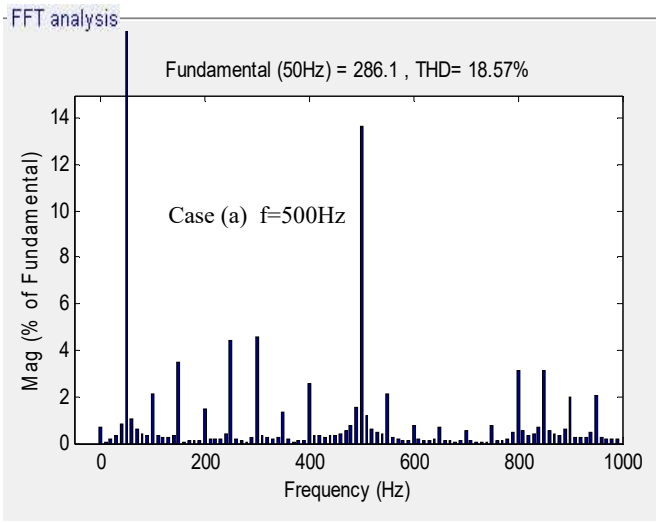
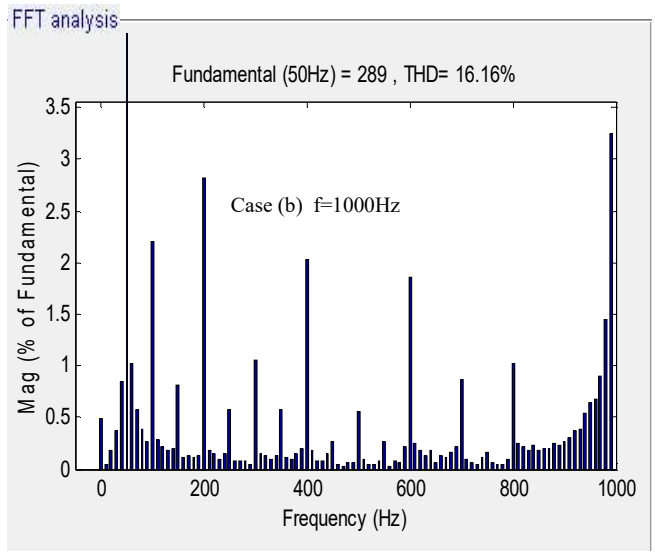


Fig. 9: THD of the voltage waveform for five level at (a) 500, (b)1000, (c)1500 Hz





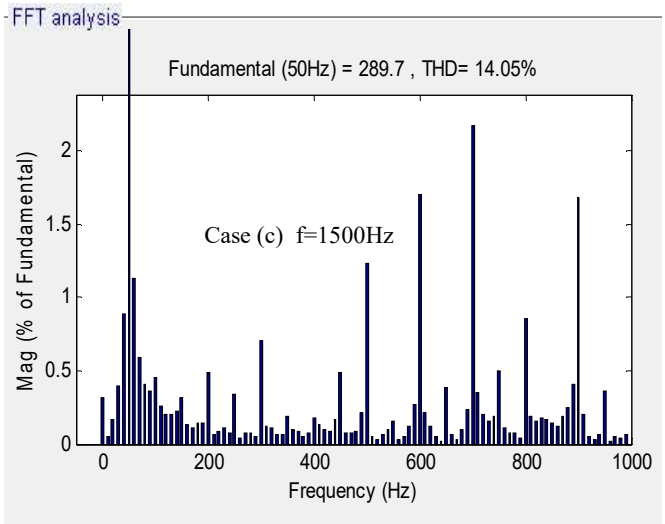


Fig.10: THD of the voltage waveform for seven level at (a) 500, (b)1000, (c)1500 Hz

Table (3) Statistical values of the THD of the voltage waveform for different cases of study with different frequencies and levels

THD (Total harmonic distortion)				Frequency (Hz)
5-level	7-level	9-level	11-level	
26.2	18.75	12.29	10.13	500 Hz
24.92	16.06	12.2	8.73	1000 Hz
21.45	14.05	10.87	7.43	1500 Hz
18.95	12.21	9.84	7.02	2000 Hz
16.13	10.76	9.13	6.3	2500 Hz
13.72	9.28	8.13	5.23	3000 Hz
11.16	7.49	7.88	4.34	3500 Hz
10.6	6.59	7.65	3.69	4000 Hz
8.13	6.3	7.12	3.1	4500 Hz
8.01	5.47	7.1	3.01	5000 Hz

On the other hand, this leads to improved THD values with increasing switching frequency, although it also increases power switching losses [15,16]. The FFT results for the five-level, seven-level, nine-level, and eleven-level multilevel inverters provide the total harmonic distortion for the four configurations as the switching frequency varies, as shown in Table (3).From this results it can be deduced that the THD of the multi-level cascaded H-bridge inverters can operate satisfactory according to with the IIEEE 519 – 2014 standard for Harmonic for proper switching frequency. Overall, the switching frequency significantly affects the performance and efficiency of cascaded multilevel inverters, making it essential to optimize this frequency according to the specific requirements of the application.

VIII- CONCLUSIONS

This paper examines the effects of increasing levels and switching frequency on the total harmonic distortion (THD) in multilevel inverters (MLCIs). It concludes that higher levels and switching frequencies reduce THD, improving output quality. However, switching frequency also impacts system efficiency, component stress, control complexity, and electromagnetic interference (EMI). Therefore, selecting the optimal frequency requires balancing power quality, efficiency, thermal management, size, cost, noise, and control complexity. The ideal frequency depends on the specific requirements and constraints of the application, aiming to optimize performance while minimizing.

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